IN THE CLAIMS:

Claims 1-6 (Canceled).

Claim 7 (Currently Amended): A liquid crystal display device comprising:

first and second substrates facing into each other;

a gate line on the first substrate;

a gate insulating layer on the first substrate including the gate line;

an active layer on the gate insulating layer;

a data line over the active layer;

a passivation layer on the data line;

a pixel electrode on the gate insulating layer and having a stitch line therein, the stitch line corresponding to a boundary line defined by different exposures during a step-and-repeat process for forming the passivation layer; and

a black matrix over the second substrate,

wherein the stitch line in the pixel electrode substantially overlaps the black matrix in a vertical direction.

Claim 8 (Currently Amended): A liquid crystal display device comprising:

first and second substrates facing into each other;

a gate line on an inner surface of the first substrate;

a first insulating layer on the gate line;

a silicon layer on the first insulating layer;

a data line on the silicon layer, the data line crossing the gate line;

a second insulating layer on the data line, the second insulating layer having the same shape as the silicon layer;

a pixel electrode at a pixel region defined by the gate and data lines;

a black matrix on an inner surface of the second substrate;

a common electrode on the black matrix; and

a liquid crystal layer between the first and second substrates, wherein at least one stitch line is formed in the ~~gate~~ first insulating layer during a step-and-repeat exposure for forming the second insulating layer, and the black matrix substantially overlaps the stitch line in a vertical direction.

Claim 9 (New): The device according to claim 8, wherein the stitch line is disposed over the gate line and the data line.

Claim 10 (New): The device according to claim 7, wherein the stitch line is disposed over the gate line and the data line.

Claim 11 (New): The device according to claim 7, wherein the gate insulating layer has the stitch line therein.